Resume

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Research interests

High performance computer architecture, multi-core multi-threaded micro-architecture, Network-On-Chip (NOC), adaptive architecture, power-aware micro-architecture, high performance computing, parallel computing, Cloud computing, Big Data, architecture modeling and simulation, performance evaluation.

Academic Background

1- **Ph.D** in Computer Architecture, Electrical and Computer Engineering, University of Rochester (NY), October 2005. Advisor: **Prof. David Albonesi**. Thesis title: "Highly Efficient Multi-Threaded Architecture".
M.S. in Electrical and Computer Engineering, University of Rochester (NY), May 2002, Courses include: Computer Architecture, Digital Integrated Circuit Design, VLSI Design Project, Data and Computer Communications, Operating Systems. **GPA:** 3.914 / 4.000

2- **M.S.** in Electronics and Communications Engineering at Faculty of Engineering, Cairo University, June 2000 Thesis title: "Fail-aware clock synchronization algorithm for real-time distributed systems". Courses included: Computer networks, Computer architecture, Pattern and speech recognition, Information systems, Real-time systems, Numerical analysis, Technical English.

3- **B.S.** in Electronics & Communications Department, Faculty of Engineering, Cairo University (Honors), July 1996. Majored in Computers & Systems.

Professional Background

01/2017-current
Associate Professor, Electrical & Computer Engineering Dept., University of Sharjah, Sharjah, UAE.

09/2010-01/2017
Assistant Professor, Electrical & Computer Engineering Dept., University of Sharjah, Sharjah, UAE.

01/2010-08/2010
Senior Software Developer at GRD Egypt DVT Modelsim Team, Mentor Graphics Egypt, Cairo, Egypt. .

02/2007-01/2010
Advisory R&D engineer at Advanced Technology & Center for Advanced Studies Dept. at IBM Cairo Technology Development Center (CTDC), Cairo, Egypt.

02/2007-08/2010
Researcher (Teacher) at the Dept. of Computer and Systems at the Electronics Research Institute (ERI), Cairo, Egypt. Member of the parallel processing & distributed systems research group.

08/2005- 10/2007

Software engineer at Architecture Performance & Projection Team at Software Solution Group at Intel Corporation, Santa Clara (CA).

06/2001- 08/2005

Research Assistant with Prof. David Albonesi in the Dept. of ECE, University of Rochester (NY).

05/2003- 11/2003

Architecture engineer at Oregon Design Center-Enterprise Processor Devision (ODC-EPD) at Intel Corporation, Hillsboro (OR), Member of Architecture Design team. Rating: Outstanding.

02/2003

Training regarding the LPX prototype and the design methodology for the S/390 Parallel Enterprise Server G4, at IBM T.J. Watson Research Center, Yorktown Heights, NY.

09/2000- 06/2001

Teaching Assistant at the Dept. of ECE, University of Rochester (NY), for Logic Design and C++ Programming Language courses.

02/1999- 08/2000

Research Assistant at the Dept. of Computer and Systems at the Electronics Research Institute (ERI), Cairo, Egypt. Member of the parallel processing & distributed systems research group.

• Professional Skills

1- MPI programming for Cluster Computers / Supercomputers (i.e. IBM Blue Gene Series)
2- STI Cell Processor programming model & coding.
3- IBM POWER processor series Instruction Set Architecture (ISA).
4- Assembly language programming.
5- Multi-Threaded/ Multi-Core Processor performance and power modeling.
6- C/C++ & Object Oriented programming under Unix & using Windows SDK & MS VisualStudio.
7- Multithreaded programming including different synchronization techniques (Mutex, Event).
8- Network programming using sockets.
9- Programming on a Shared Memory Network Using SCRAMNet Library.
10- Working knowledge of ModelSim for Verilog Simulation & Functional coverage
11- VLSI design and Simulation Using Cadence and Verilog.
12- Circuit Design using ALTERA MAX+ Plus II V. 9.4 and VHDL.
13- Working knowledge of UNIX on SUN Solaris Workstation and Perl scripts.

• Projects

1- "*Advanced Signal Processing Algorithms and Performance Analysis for Next Generation Wireless Systems*" **University of Sharjah,** Research Institute For Science and Engineering, Research Grant.
2- "*Optimal Resource Management for Cloud-Based Fifth Generation Wireless Networks*" **University of Sharjah,** Research Institute For Science and Engineering, Research Grant no. 1602040336-P.
3- "*Scalable Job Scheduling & Resource Allocation for Highly Efficient Multi-threaded Multi-core Processors*" **University of Sharjah** Seed Grant no. 110223.
4- Functional Coverage Modeling and Design for ModelSim circuit Simulator of **Mentor Graphics-Cairo**, February 2010.
5- Parallel implementation using MPI for Computational intensive modules for NanoTechnology Applications (IBM Blue Gene/L), July 2009, **IBM**.
6- High Performance Computing Application for 3D CTScan Medical Imaging machines (STI Cell Processor), September 2008, **IBM**.
7- Implementation for ISA simulation on IBM Mambo simulator (IBM POWER7 Processor), March 2008.
8- 3D transpose for multi-core processors with software managed memory hierarchy (STI Cell Processor), June 2007, **IBM**.
9- Multi-threaded Workload Phase Detection & Classification (Intel Mobile & Desktop Core Processors), Feb. 2007, **Intel**.
10- Dynamically Tunable Clustered Multithreaded Architectures (academic research), July 2005, **University**

of Rochester.

11- MP Server Modeling & Simulation (Intel Xeon Processors), Nov. 2003, **Intel**.

12- "1-V ADPSM Processor for Low-Power Wireless Applications" & "Floating-Point Adder": A VLSI Design project, designed using Cadence, and as a requirement for a course on VLSI, Dec. 2000 & May 2001, **University of Rochester**.

• Publications

• Journals:

- Wael S. Afifi, **Ali A. El-Moursy**, Mohamed Saad, Hadia ElHenawi, and Salwa M. Nassar, *"A Novel Scheduling Technique for Improving Cell-edge Performance in 4G/5G Systems"*, Submitted.
- **Ali A. El-Moursy**, Saeed Abdallah, Mohamed Saad, and Khawla Alnajjar, *"Parallel Two-Way Relay Channel Estimation in Cloud-based 5G Radio Access Networks"*, Submitted.
- **Ali A. El-Moursy**, Ahmed S. S. Mohamed, Magdy A. El-Moursy, "*Real-Time Memory Controller for Embedded Multi-core System"*, Journal of Systems Architecture, Elsevier, Submitted.
- **Ali A. El-Moursy**, Amany Abdelsamea, Rukshanda Kamran and Mohamed Saad, "*Multi-Dimensional Regression Host Utilization algorithm (MDRHU) for Host Overload Detection in Cloud Computing"*, Journal of Cloud Computing: Advances, Systems and Applications, Springer, Accepted (April 2019).
- Sayed T Muhammad, Mohamed Saad, **Ali El-Moursy**, Magdy A El-Moursy, Hesham F Hamed, "*CFPA: Congestion aware, fault tolerant and process variation aware adaptive routing algorithm for asynchronous Networks-on-Chip"*, Journal of Parallel and Distributed Computing, Elsevier, Volume 128, June 2019: 151-166 (2019).
- **Ali A. El-Moursy**, Amr S. Elhelw*, "Adaptive TB-LMI: An Efficient Memory Controller and Scheduler Design"*, Concurrency And Computation: Practice And Experience, 31(7) (2019).
- Abdelsamea, A., **El-Moursy, A. A.**, Hemayed, E. E., & Eldeeb, H., "*Virtual Machine Consolidation Enhancement using Hybrid Regression Algorithms*", Egyptian Informatics Journal**, 18(3) (2017): 161-170.**
- Sayed T Muhammad, Magdy A El-Moursy, **Ali El-Moursy**, Hesham F Hamed, "*Architecture Level Analysis for Process Variation in Synchronous and Asynchronous Networks-on-Chip"*, Journal of Parallel and Distributed Computing, 102(1): 175–185 (2017).
- **Ali A. El-Moursy**, Wael S. Afifi, Fadi N. Sibai and Salwa M. Nassar, *"Parallel PPI Prediction Performance Study on HPC Platforms"*, Journal of Circuits, Systems, and Computers, 24(5): 1-28 (2015).
- **Ali A. El-Moursy**, Walid El-Reedy, Hossam A. H. Fahmy, "*Fair memory access scheduling algorithms for multicore processors"*, International Journal of Parallel, Emergent and Distributed Systems, Taylor & Francis Group, 30(4): 286-308 (2015).
- Sayed T. Muhammad, Rabab Ezz-Eldin, Magdy A. El-Moursy, **Ali A. El-Moursy**, Amr M. Refaat, "*Traffic-Based Virtual Channel Activation for Low-Power NoC"*, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 23(12): 3029-3042 (2015).
- **Ali A. El-Moursy**, Fadi N. Sibai, "*V-Set Cache: An Efficient Adaptive Shared Cache For Multi-Core Processors"*, Journal of Circuits, Systems, and Computers, 23(7): 1-28 (2014).
- **Ali A. El-Moursy**, Hanan ElAzhary, Akmal Younis, "*High-accuracy hierarchical parallel technique for hidden Markov model-based 3D magnetic resonance image brain segmentation"*, Concurrency and Computation: Practice and Experience, J. Wiley, 26(1): 194-216 (2014).
- Fadi N. Sibai, **Ali A. El-Moursy**, "*Performance evaluation and comparison of parallel conjugate gradient on modern multi-core accelerator and massively parallel systems"*, International Journal of Parallel, Emergent and Distributed Systems, Taylor & Francis Group, IJPEDS 29(1): 38-67 (2014).
- **Ali A. El-Moursy**, Sheif Saif, Akmal Younis, "*Hierarchical-based parallel technique for HMM 3D MRI brain segmentation algorithm"*, International Journal of Parallel, Emergent and Distributed Systems, Taylor & Francis Group, IJPEDS 27(4): 297-316 (2012).
- **Ali A. El-Moursy**, Fadi N. Sibai, "*Image Processing Applications Performance Study On Cell BE And Blue Gene/L"*, Concurrency And Computation: Practice And Experience, J. Wiley, Volume 23,

Issue 4, pages 351–371, 25 March 2011.

- **Conferences:**

- Hanan Khaled, **Ali A. ElMoursy**, Salwa Nassar, Mohamed Taher, Fadi Sibai, "*Parallel Study of 3-D Oil Reservoir Data Visualization Tool Using Hybrid Distributed/Shared-Memory Models",* The Fourth IEEE International Conference on Big Data Intelligence and Computing (IEEE DataCom 2018), Athens, Greece, pages: 1016-1021, August 2018.
- Sayed T. Muhammad, **Ali A. El-Moursy**, Magdy A. El-Moursy, Hesham F. A. Hamed, "*System-level simulator for process variation influenced synchronous and asynchronous NoCs",* 30th IEEE International System-on-Chip Conference (SOCC 2017), Munich, Germany, pages: 298-302, September 2017.
- Amany Abdelsamea, **Ali A. El-Moursy**, Elsayed E. Hemayed, Hesham Eldeeb, "Multiple Regression Host Overload Detection Algorithm" , Accepted, Proc. Sensors to Cloud Architectures Workshop (SCAW), in conjunction with The 22nd International Symposium on High-Performance Computer Architecture (HPCA-22), Barcelona, Spain, March 12-16, 2016.
- Amr S. Elhelw, **Ali El Moursy**, Hossam A. H. Fahmy, "*Adaptive Time-Based Least Memory Intensive scheduling",* IEEE 9th International Symposium on Embedded Multicore/Manycore SoCs (MCSoc 2015), Turin, Italy, pages 167-174, September 23-25, 2015.
- Ahmed S. S. Mohamed, **Ali A. El-Moursy**, , Hossam A. H. Fahmy, "*Real-Time Memory Controller for Embedded Multi-core System"*, In the Proceeding of the 17th International Conferences on High Performance Computing and Communications (HPCC-2015), New York, USA, pages 839-842, August 24 - 26, 2015.
- S. T. Muhammad, M. A. El-Moursy, **A. A. El-Moursy**, and A. M. Refaat, "Optimization for Traffic-Based Virtual Channel Activation Low-Power NoC", Proceedings of the 5th IEEE International Conferences on Energy Aware Computing Systems and Applications, Cairo, Egypt, pages 1-4, 24-26 March, 2015.
- **Ali A. El-Moursy**, *"Adaptive V-Set Cache for Multi-core Processors"*, IEEE 8th International Symposium on Embedded Multicore/Manycore SoCs (MCSoc 2014), Aizu-Wakamatsu, Japan, pages 297-302, 23-25 Sept. 2014.
- Amr S. Elhelw, **Ali El Moursy**, Hossam A. H. Fahmy, *"Time-Based Least Memory Intensive Scheduling"*, IEEE 8th International Symposium on Embedded Multicore/Manycore SoCs (MCSoc 2014), Aizu-Wakamatsu, Japan, pages 311-318, 23-25 Sept. 2014.
- Sayed T. Muhammad, Magdy A. El-Moursy, **Ali A. El-Moursy**, Amr M. Refaat, *"Traffic-Based Virtual Channel Activation for Low-Power NOC"*, the 8th International Design and Test Symposium (IDT), pages 1-6, December 16-18, 2013 (**Best Paper Award**).
- Wael S. Afifi, **Ali A. El-Moursy**, Salwa Nassar, M. A. Mohamed, Fadi N. Sibai, "*Parallel Protein Sequence Matching using HPC"*, International Conference of Information Science and Computer Applications (ICISCA 2012), Bali, Indonesia, November 19-20, 2012.
- Walid El-Reedy, **Ali El-Moursy**, Hossam A. H. Fahmy, *"High Performance Memory Requests Scheduling Technique for Multicore Processors"*, In the Proceeding of High Performance Computing and Communication & 2012 IEEE 9th International Conference on Embedded Software and Systems (HPCC-ICESS), 2012 IEEE 14th International Conference on, pp. 127-134, June 2012 (IEEE Conference).
- **Ali El-Moursy**, and Fadi N. Sibai, *"V-Set Cache Design for LLC of Multi-core Processors"*, In the Proceeding of High Performance Computing and Communication & 2012 IEEE 9th International Conference on Embedded Software and Systems (HPCC-ICESS), 2012 IEEE 14th International Conference on, pp. 995-1000, June 2012 (IEEE Conference).
- Fadi N. Sibai, **Ali El-Moursy**, Nader Mohamed, *"Throughput and Latency Analysis of the Spidergon-Donut Interconnection Network"*, The Eighth International Conference on Innovations in Information Technology (Innovations'12), pp. 356-360, March 2012 (IEEE Conference).
- Ahmed Sayed, **Ali El-Moursy**, Hisham El-Shishiny, *"Scalability Of Abinit On Blue Gene/L For Identifying Band Structures For Nanotechnology Materials"*, The 2nd International Conference On Advanced Computer Theory And Engineering (ICACTE-2009) (IEEE Conference), pp. 1437-1444.
- **Ali El-Moursy**, Ahmed El-Mahdy, Hisham El-Shishiny, *"An Efficient in-Place 3D Transpose for*

Multicore Processors with Software Managed Memory Hierarchy", International Forum on Next-Generation Multicore/Manycore Technologies (IFMT-2008) (IEEE-ACM Conference).

- **A. El-Moursy**, R. Garg, D.H. Albonesi and S. Dwarkadas, *"Compatible Phase Thread Co-Scheduling for a CMP of SMT Processor"*, IEEE International Parallel & Distributed Processing Symposium (IPDPS-2006).
- R. Garg, **A. El-Moursy**, S. Dwarkadas, D.H. Albonesi, J. A. Rivers and V. Srinivasan, *"Cache Design Options for a Clustered Multithreaded Architecture"*, Technical Report 866, University of Rochester, Computer Science Department, UR CSD / TR 866, October 2005.
- **A. El-Moursy**, R. Garg, D.H. Albonesi and S. Dwarkadas, *"Partitioning Multi-Threaded Processors with Large Number of Threads"*, IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS-2005).
- **A. El-Moursy** and D.H. Albonesi, *"Front-End Policies for Improved Issue Efficiency in SMT Processors"*, 9th International Symposium on High-Performance Computer Architecture.
- Martin Margala, Magdy A. El-Moursy, **Ali El-Moursy**, Junmou Zhang, Wendi Heinzelman, *"1-V ADPCM Processor for Low-Power Wireless Applications"*, VLSI-SOC 2003: 386-393
- A. Buyuktosunoglu, **A. El-Moursy**, and D.H. Albonesi, "*An Oldest-First Selection Logic Implementation for Non-Compacting Issue Queues"*, 15th International ASIC/SOC Conference.

- **Patents:**

- Hisham El-Shishiny, **Ali El-Moursy**, "*Equal duration and equal fetch operations sub-context switch interval based fetch operation scheduling utilizing fetch error rate based logic for switching between plurality of sorting algorithms*", US Patent 8640133, January 28, 2014.
- **Ali A. El-Moursy**, Hisham El-Shishiny, Ahmed T. Sayed Gamal El Din, *"Scheduling Threads"*, US Patent 20120192195, July 26, 2012.
- Ahmed El-Mahdy, **Ali El-Moursy**, Hisham El-Shishiny, *"Multi-Core Processors For 3D Array Transposition By Logically Retrieving In-Place Physically"*, US Patent 7979672, July 12, 2011.
- **Ali El-Moursy**, Hisham El-Shishiny, *"Method and System for Job Scheduling"*, US Patent US 2011/0004883 A1, 06 Jan. 2011.
- Hisham El-Shishiny, **Ali El-Moursy**, *"Fetch Operation Scheduling"*, US Patent US 2010/0162041 A1, 24 June 2010.
- Ahmed H.m.r. El-Mahdy, **Ali A. El-Moursy**, Hisham Elshishiny, *"Method And System For In-Place Multi-Dimensional Transpose For Multi-Core Processors With Software-Managed Memory Hierarchy"*, US Patent US 20100023728, 28 January 2010.

Memberships

- Coordinator of the Distributed & Networked Systems Research Group, University of Sharjah, Operational Grant: 150410.
- IEEE Senior Member.

Teaching Courses

- Digital Logic Design – 0403201
- Digital Logic Design Lab – 0403202
- Microprocessor & Assembly Language – 0403230
- Microprocessor & Assembly Language Lab – 0403231
- Computer System Architecture – 0403326
- Parallel & Distribute Processing – 0403412
- Random Signal Theory -- 0402241
- Microcontroller Based Design Lab – 0403337
- Engineering Ethics – 0403300
- Computer Architecture (Graduate level) – 0403520

Referee

- Editor, Microelectronics Journal, Elsevier
- Associate Editor, Journal of Circuits, Systems, and Computers, World Scientific
- Reviewer, IEEE Transactions on Parallel and Distributed Systems, IEEE
- Reviewer, IEEE Transactions on Architecture and Code Optimization, IEEE
- Reviewer, Journal of Parallel and Distributed Computing, Elsevier Inc.
- Reviewer, Journal of Neural Computing and Applications, Springer.
- Reviewer, International Journal of Circuit Theory and Application, John Wiley & Sons, Ltd.
- Reviewer, Computing Journal, Springer.
- TPC Member, The International Conference on Advanced Information Networking and Applications (AINA-2016)
- TPC Member, - The 7th International Conference on Computer Science and Information Technology (CSIT 2016)
- TPC Member, 7th International Forum on Engineering Education (IFEE2015) Quality Assurance in Engineering Education
- Reviewer, IEEE International Symposium on Circuits and Systems (ISCAS 2011- 2017)
- Reviewer, The ANNUAL IEEE/ACM International Symposium on Microarchitecture
- Workshop on Complexity-Effective Design in conjunction with the 31st International Symposium on Computer Architecture

References

- Prof. Ashraf Salem: Senior Engineering Director, **Mentor Graphics** Corporation, Cairo, Egypt.
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- Dr. Hisham El-Shishiny: Department Manager, Advanced Technology & Center for Advanced Studies Dept. at **IBM** Cairo Technology Development Center (CTDC), Cairo, Egypt.
  - Email:shishiny@eg.ibm.com Tel: (202) 3536-1461
- Baqar Zaidi: Projection Manager, Performance Tracing & Technology-Software Solution Group (PTT-SSG), **Intel** Corporation, California, USA.
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- Prof. David H. Albonesi: Computer Systems Laboratory at **Cornell University**, 14853, Ithaca, New York, USA.
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- Prof. Sandhya Dwarkadas: Department of Computer Science at **University of Rochester**, Rochester, NY 14627-0226.
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- Ganapati Srinivasa: Architecture Manager, Oregon Design Center-Enterprise Processor Division (ODC-EPD), **Intel** Corporation.
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